Recent Advances in High-Speed and Large-Swing Integrated Circuits Implemented in InGaAs and GaAsSb InP DHBT for Terabit-Class Optical Communications

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ESSDERC – ESSCIRC Workshop
the 22nd of September 2021

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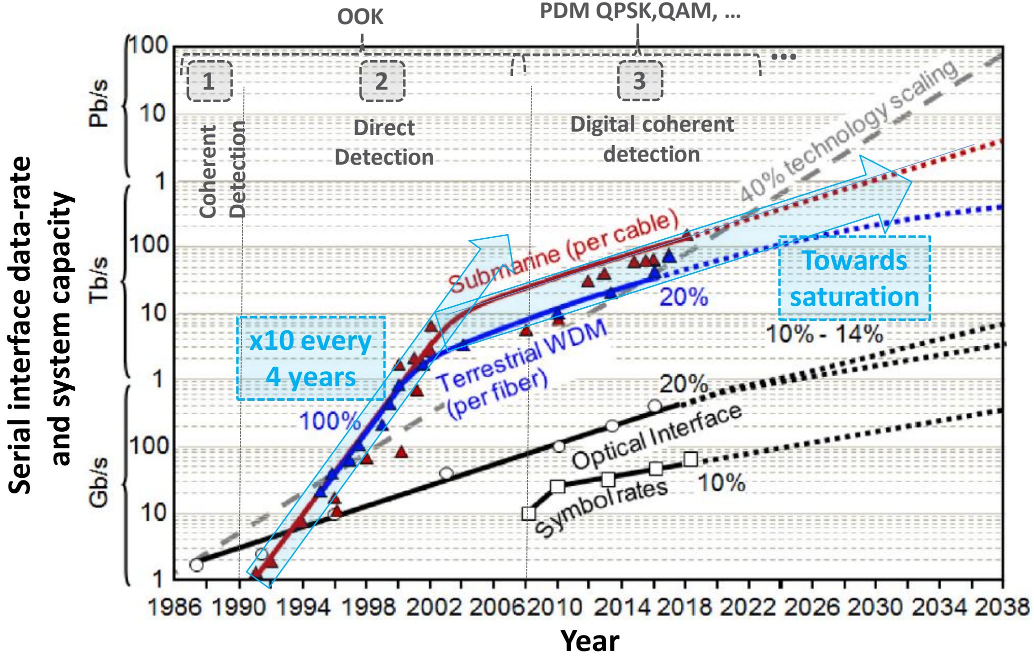
Optical systems capacity evolution: 1980-2018+



Source : P. J. Winzer et al. Fiber-optic transmission and networking : the previous 20 and the next 20 years. Optics Express, Sept. 2018

Bandwidth hungry applications:

Video streaming

Internet of things (*IoT*)

Cloud computing

5G

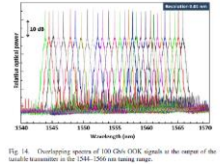
…

Optical system's capacity is heading towards saturation and cannot support tomorrow's IP traffic

How can we increase the optical capacity?

$$C = D_S \,.\, \log_2(N_S) \,.\, N_\lambda \,.\, N_{pol}$$

> 1 Tb/s/chanel



Space

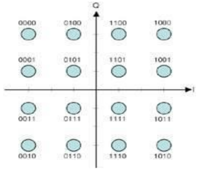
Optical channel and light polarisation

Requires a higher **optical bandwidth**

Optical Network Capacity

Spectral efficiency

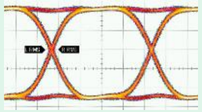
Complex Modulation format



Requires higher **linearity** and **SNR**

Spectrum

Electrical Symbol-Rate



43-Gb/s InP DFF - Konczykowska et al. 2009 - rms jitter=234 fs, S/N=46

Requires a higher **electrical bandwidh**

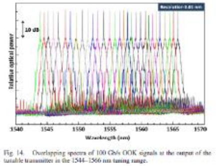
> 125 GBd

1st focus: Increasing the electrical symbol-rate to increase the optical capacity

How can we increase the optical capacity?

$$C = D_S \,.\, \log_2(N_S) \,.\, N_\lambda \,.\, N_{pol}$$

> 1 Tb/s/channel

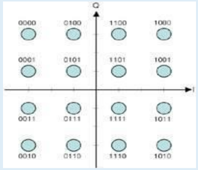


Space
Optical channel and light polarisation

Requires a higher
optical bandwidth

Optical Network Capacity

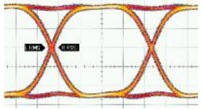
Spectral efficiency
Complex Modulation format



Requires higher
linearity and **SNR**

16-QAM (PAM-4)

Spectrum
Electrical Symbol-Rate



43-Gb/s InP DFF - Konczykowska et al. 2009 - rms jitter=234 fs, S/N=46

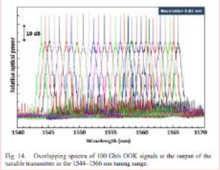
Requires a higher
electrical bandwidh

2nd focus: Increasing the spectral efficiency to increase the optical capacity

How can we increase the optical capacity?

$C = D_S \,.\, \log_2(N_S) \,.\, N_\lambda \,.\, N_{pol}$

> 1 Tb/s/channel



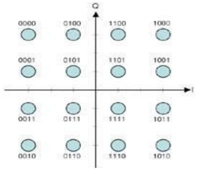
Space
Optical channel and light polarisation

Requires a higher
optical bandwidth

Both light polarisations

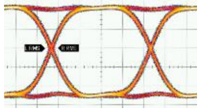
Optical Network Capacity

Spectral efficiency
Complex Modulation format



Requires higher
linearity and **SNR**

Spectrum
Electrical Symbol-Rate

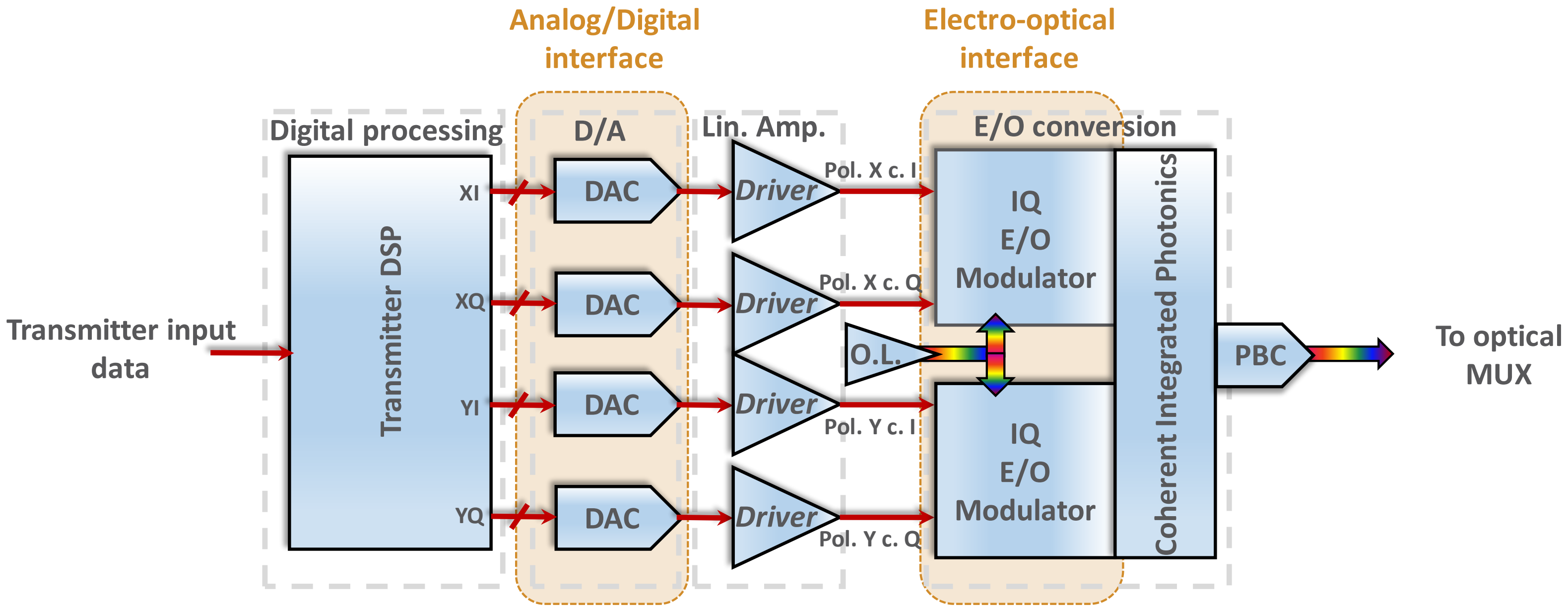


43-Gb/s InP DFF - Konczykowska et al. 2009 - rms jitter=234 fs, S/N=46

Requires a higher
electrical bandwidh

Optical devices prerogative

Current digital coherent transmitters: Tx side



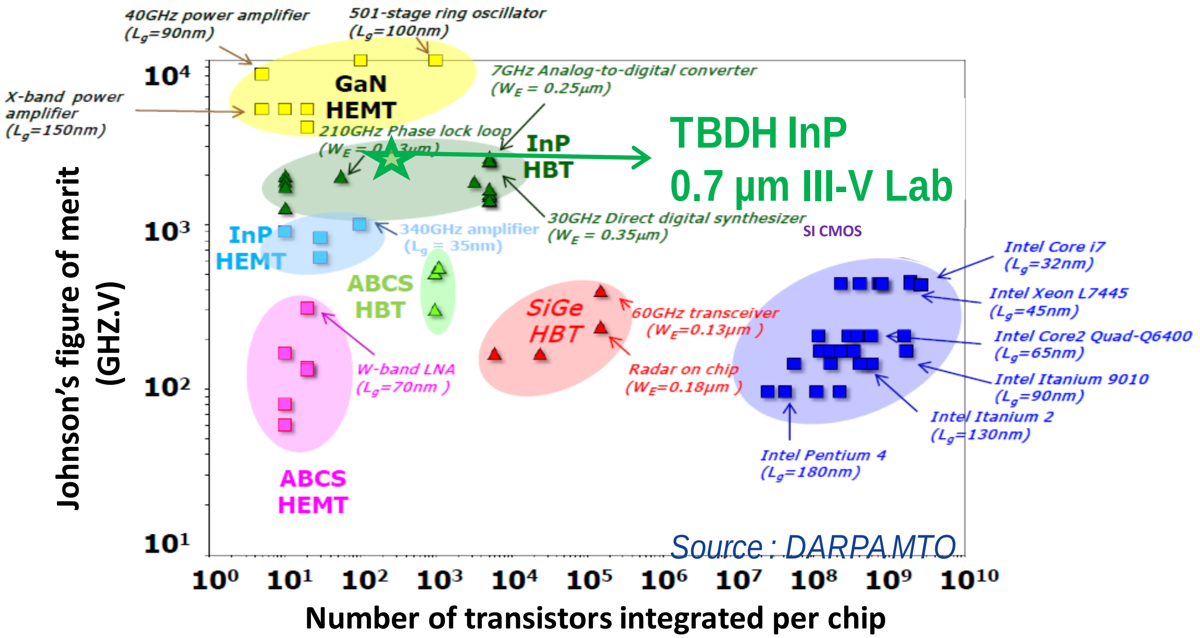
Data converts and E/O modulators are key components for digital coherent transmitters

High-speed transistors' state-of-the-art

$$FoM_{Johnson} = f_T . BV_{CE0}$$

Transition Frequency

Breakdown voltage



Terminology:
InP = indium phosphide, GaN = gallium nitride, SiGe = silicon germanium, ABCS = antimonide-based compound semiconductor
HBT = heterojunction bipolar transistor, HEMT = high electron mobility transistor, L_g = gate length, W_E = emitter width

InP DHBT technologies show among the highest speed x breakdown voltage trade-off

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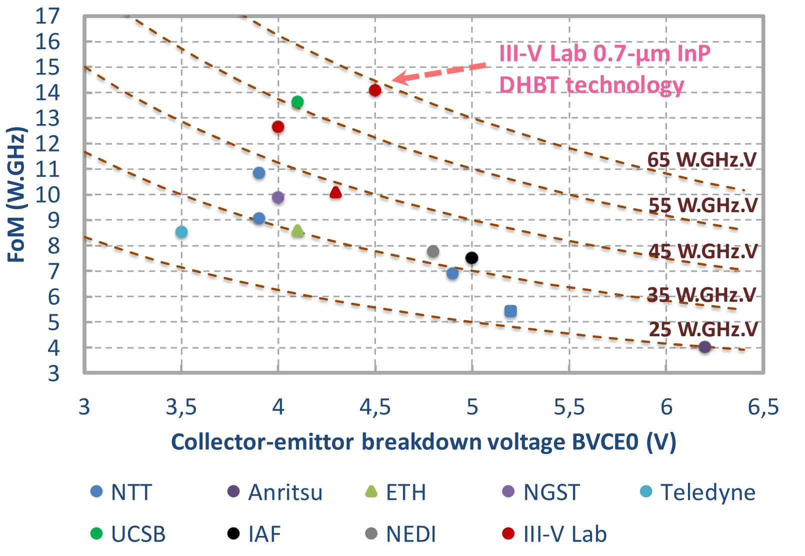
III-V Lab 0.7-µm InP DHBT technology

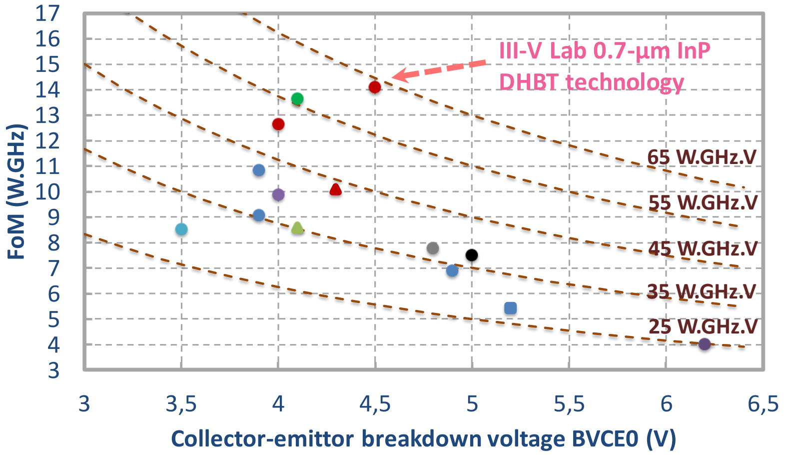


$$\text{FoM} = (f_T \cdot f_{MAX})^{1/2} \cdot (I_c \cdot V_{ce})_{@\ \text{peak}\ fT}$$

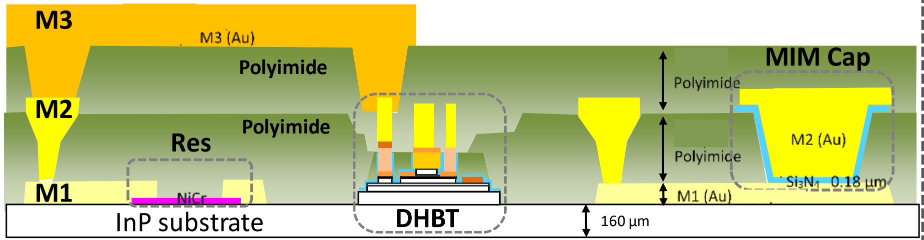
Source : V. Nodjiadjim et al. "0.7-µm InP DHBT technology with 400-GHz f_T and f_{MAX} and 4.5-V BV_{CEO} for high speed and high frequency integrated circuits". IEEE journal of the Electron Devices Society, pages 748–752, July 2019.

III-V Lab technology shows the best performances for ultra-high-symbol-rate and high output swing circuit design

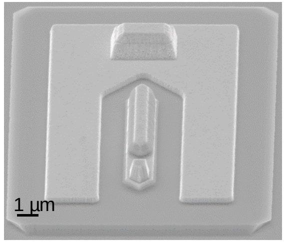
III-V Lab 0.7-µm InP DHBT technology



$$\text{FoM} = (f_T \cdot f_{MAX})^{1/2} \cdot (I_c \cdot V_{ce})_{@\,\text{peak}\,fT}$$



0.7 x 5 µm² DHBT



InP/InGaAs/InP DHBT

3 Au-based metallisation

Si_3N_4 MIM capacitors

NiCr thin film resistors

400-GHz peak f_T and f_{MAX} at J_C = 6 mA/µm²

a 30 static current gain

A 4.5-V BV_{CE0} (breakdown voltage)

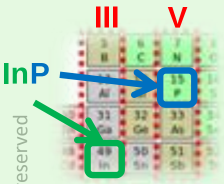
Source : V. Nodjiadjim et al. "0.7-µm InP DHBT technology with 400-GHz f_T and f_{MAX} and 4.5-V BV_{CEO} for high speed and high frequency integrated circuits". IEEE journal of the Electron Devices Society, pages 748–752, July 2019.

III-V Lab technology shows the best performances for ultra-high-symbol-rate and high output swing circuit design

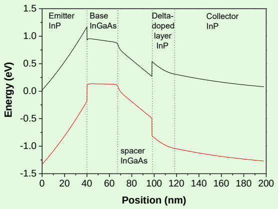
III-V Lab InP DHBT technology and activity portfolio

From nanometer…

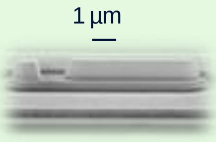
…To system in package



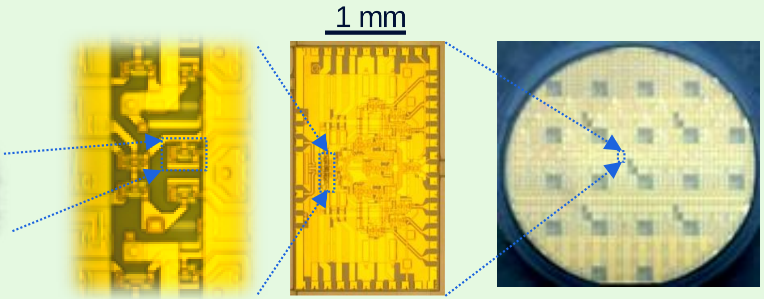
III-V materials
In: Indium
P: Phosphide



band diagram engineering through epitaxy



ultra high speed bipolar transistor



Analog-digital integrated circuits

Wafer processing

High frequency module

f_T/f_{MAX} > 400 GHz BV_{CE0} of 4.5 V	up to 250 DHBT per IC	3-inch wafer 4500 unitary chips

V. Nodjiadjim et al. "0.7-µm InP DHBT technology with 400-GHz-f_T and f_{MAX} and 4.5-V BVCE0 for high speed and high frequency integrated circuits", IEEE journal of the Electron Devices Society, pp. 748–752, July 2019

III-V Lab has the complete set of skills to develop InP based disruptive technologies

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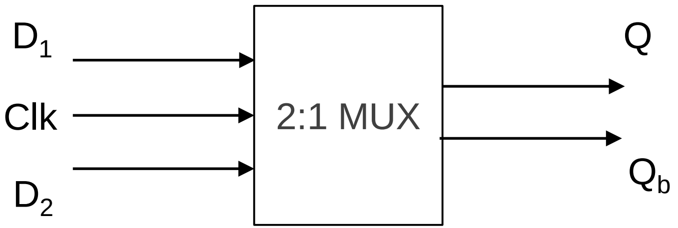
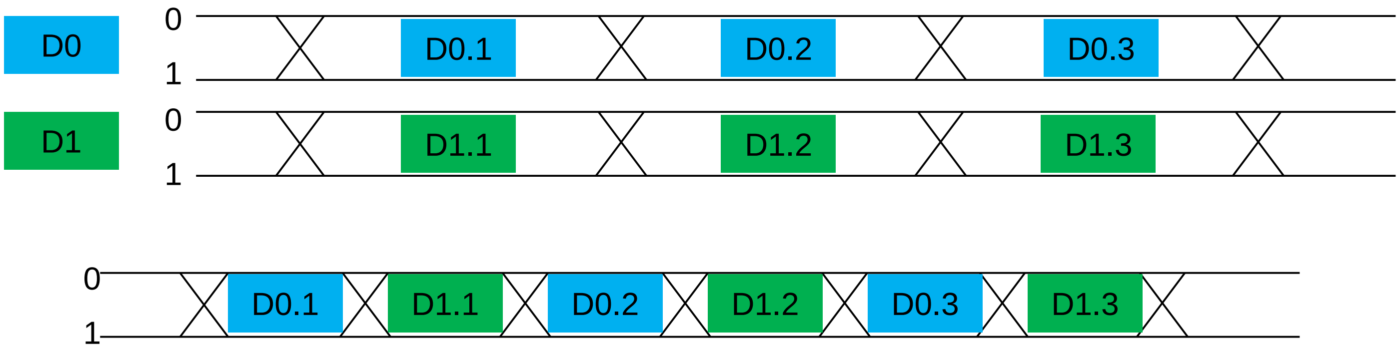
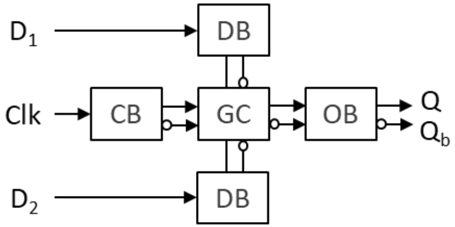
2:1 Multiplexing selector operation principle



2:1 MUX is time interleaving two input signals → *by reducing by half their time slots*



InP-DHBT 2:1 selector circuit details



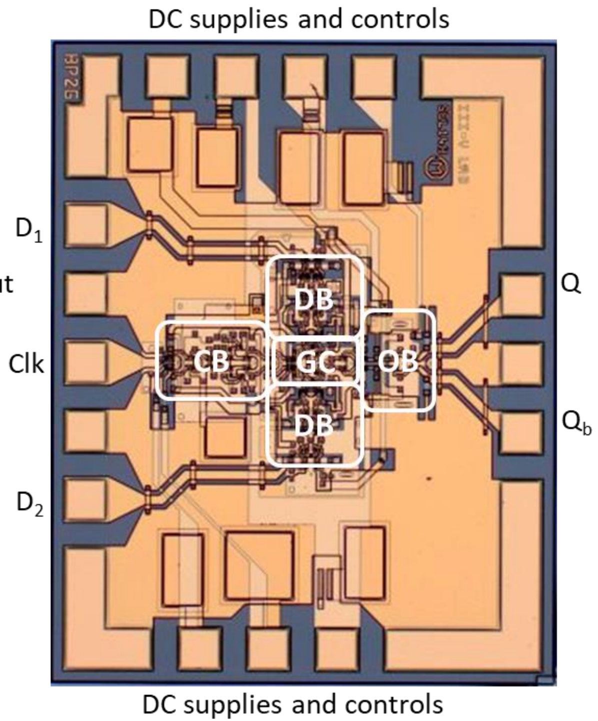
Main characteristics

- 48 transistors
- Power consumption 0.5/0.8 W for 240/730 mV diff output amplitude
- CPW RF inputs and outputs

$D_{1/2}$: 1st & 2nd input data
Clk: Clock
Q: output
Q_b: complementary output

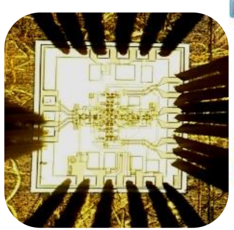
DB: Data Buffer
CB: Clock Buffer
GC: Gilbert cell
OB: Output Buffer

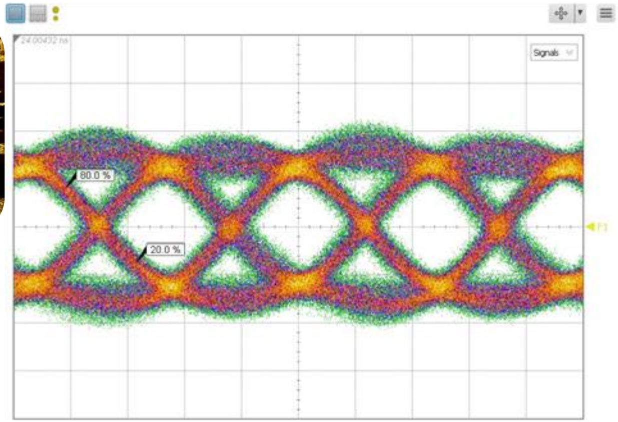
1.2×1.5 mm²



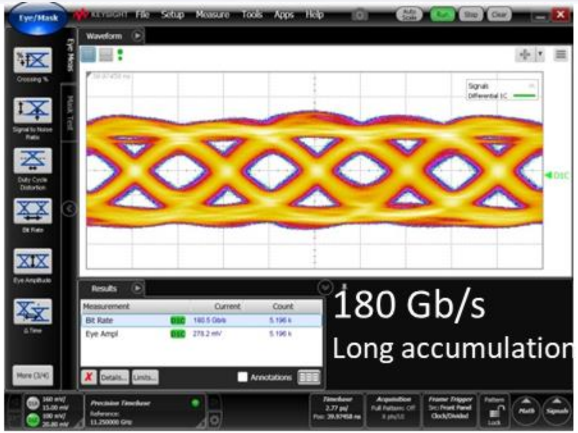
High integrability InP-DHBT multiplexing selector architecture

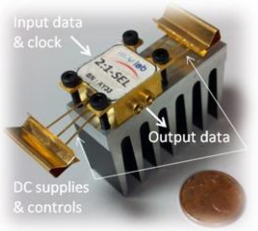
Multiplexing selector - measurements





Measurement F. Jorge (NBL)





Measurement A. Adamiecki (NBL)

World speed record
up-to **212-Gb/s**
signaling on-wafer

World speed record
up-to **180-Gb/s**
signaling in-package

InP-DHBT technology enables the highest baudrate operation

System experiments and publications

- **Electronics Letters, Jan 2019**

212-Gbit/s 2:1 multiplexing selector realised in InP DHBT

A. Konczykowska✉, F. Jorge, M. Riet, V. Nodjiadjim, B. Duval, H. Mardoyan, J.M. Estaran, A. Adamiecki, G. Raybon and J.-Y. Dupuy

- **Post-deadline Paper ECOC 2019**

222-GBAUD ON-OFF KEYING TRANSMITTER USING ULTRA-HIGH-SPEED 2:1-SELECTOR AND PLASMONIC MODULATOR ON SILICON PHOTONICS

Haïk Mardoyan[1], Filipe Jorge[2], Benedikt Baeuerle[3,4], Jose Manuel Estaran[1], Wolfgang Heni [3,4], Agnieszka Konczykowska[2], Muriel Riet[2], Bernadette Duval[2], Virginie Nodjiadjim[2], Michel Goix[2] Jean-Yves Dupuy[2], Marcel Destraz [3,4], Claudia Hoessbacher [3,4], Yuriy Fedoryshyn[4], Huajun Xu[5], Delwin Elder[5], Larry Dalton[5], Juerg Leuthold[4], Sébastien Bigo[1]

- **Post-deadline Paper ECOC 2019**

180-GBaud All-ETDM Single-Carrier Polarization Multiplexed QPSK Transmission over 4480 km

G. Raybon[(1)], A. Adamiecki[(1)], J. Cho[(1)], F. Jorge[(2)], A. Konczykowska[(2)], M. Riet[(2)], B. Duval[(2)], J.-Y. Dupuy[(2)], N. Fontaine[(1)], P. J. Winzer[(1)], S. Chandrasekhar[(1)], X. Chen[(1)]

Two different applications

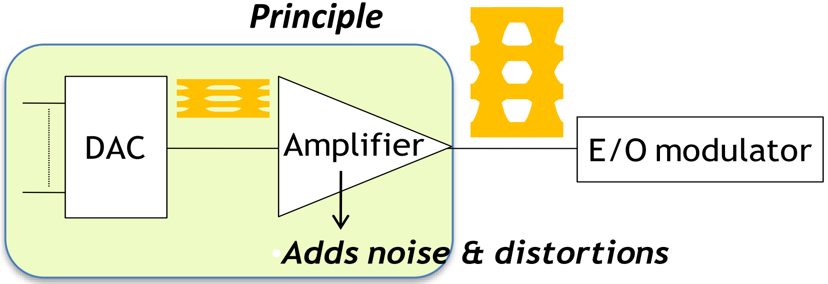
- **Data center** short range OOK with direct detection (DD) – capacity 222 Gb/s
- **Long-haul** with QPSK format and coherent receiver – capacity 4x180=720 Gb/s

High-rank publications of this InP DHBT 2:1 digital selector

Power-DAC for large swing multilevel signals – Concept

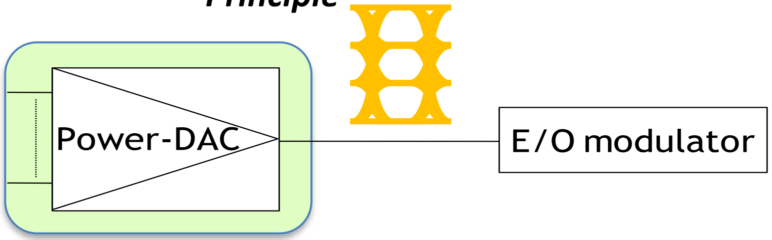
❖ DAC + linear driver (classical approach)

Principle



❖ Power-DAC (new concept)

Principle



Motivation

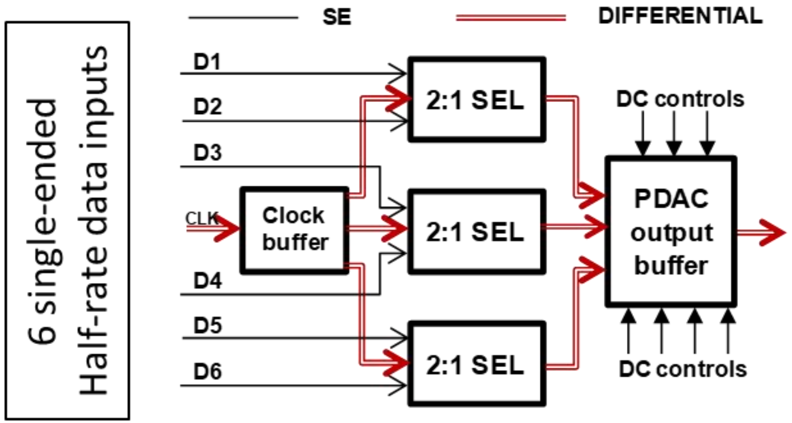
<u>Multilevel formats to increase</u>

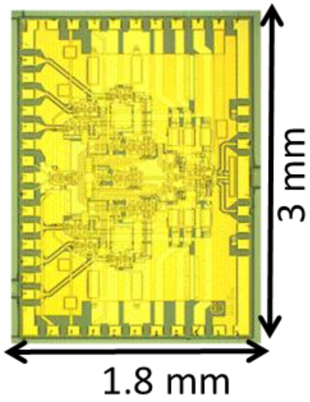
- transmission capacity and
- spectral efficiency

Power-DAC combines DAC and driver functionalities

3-bit Selector-Power-DAC

- 6 NRZ input data signals are multiplexed to obtain 3 double bitrate signals
- 3 multiplexed signals are combined and amplified to obtain PAM-8 high swing output





Power consumption
2.9 W max

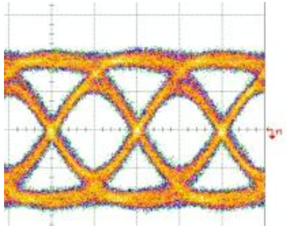
Complexity
150 transistors

Compact realisation of 2 functionalities

SPDAC3B measurements

Circuit measurements in PAM-2, PAM-4 and PAM-8 mode

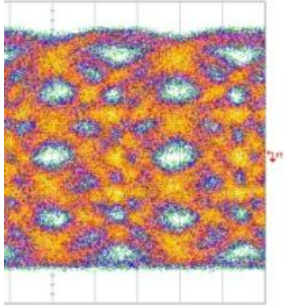
100 GBd
(100 Gb/s)



2.1 V_{ppdiff}

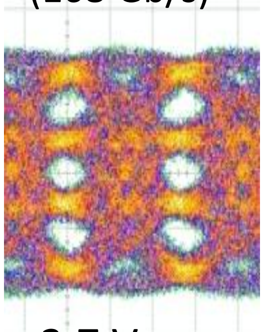
1 bit on: NRZ

100 GBd
(200 Gb/s)



3.7 V_{ppdiff}

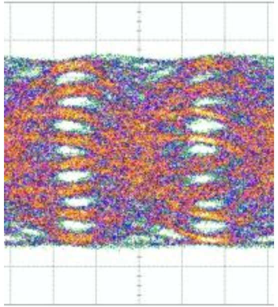
84 GBd
(168 Gb/s)



3.7 V_{ppdiff}

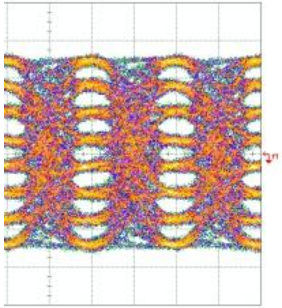
2 bits on: PAM-4

64 GBd
(192 Gb/s)



4.3 V_{ppdiff}

50 GBd
(150 Gb/s)



4.2 V_{ppdiff}

3 bits on: PAM-8

Up to 192 Gb/s signal with a 4.3-V_{ppdiff} output swing

GRENOBLE 2021 ESSDERC ESSCIRC NOKIA leti ceatech THALES

Publications and experiments

Electronics Letters

84 GBd (168 Gbit/s) PAM-4 3.7 V_{pp} power DAC in InP DHBT for short reach and long haul optical networks

A. Konczykowska✉, F. Jorge, J-Y. Dupuy, M. Riet, V. Nodjiadjim, H. Aubry and A. Adamiecki

IET AWARDS The Institution of Engineering and Technology | PREMIUM AWARD WINNER 2017

IEEE Photonic Conference (IPC), 2015

- Single Carrier All-ETDM 1.08 Terabit/s Line Rate PDM-64-QAM Transmitter Using a High-Speed Multiplexing DAC

ECOC 2016

Artificial Neural Networks for Linear and Non-Linear Impairment Mitigation in High-Baudrate IM/DD Systems

J. Estarán[(1)], R. Rios-Müller[(1)], M. A. Mestre[(1)], F. Jorge[(2)], H. Mardoyan[(1)], A. Konczykowska[(2)], J.-Y. Dupuy[(2)], and S. Bigo[(1)]

...

Many world-first experiments enabled with Power-DAC circuits

First 1 Terabit system experiment

WORLD 1st

Single-Carrier All-ETDM 1.08-Terabit/s Line Rate PDM-64-QAM Transmitter Using a High-Speed 3-Bit Multiplexing DAC

G. Raybon[1], A. Adamiecki[1], J. Cho[1], P. Winzer[1], A. Konczykowska[2], F. Jorge[2], J-Y. Dupuy[2], M. Riet[2], B. Duval[2], K. Kim[1], S. Randel[1], D. Pilori[1], B. Guan[3], N. Fontaine[1], E. C. Burrows[1]

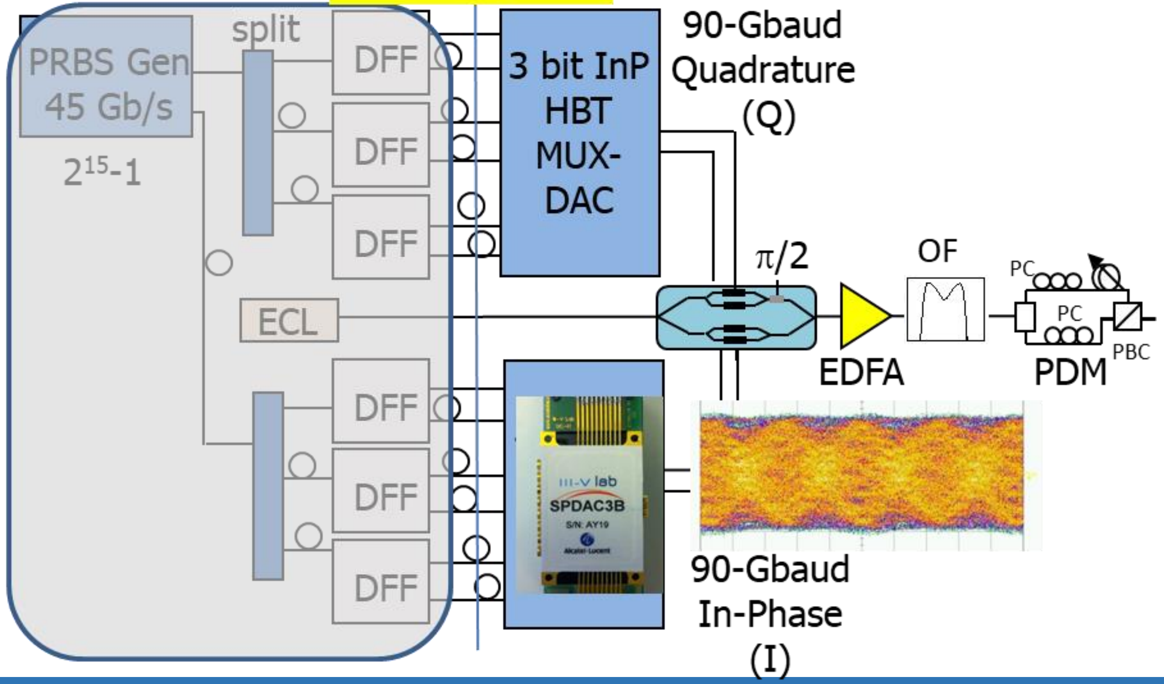
[1] Alcatel-Lucent, Bell Labs, 791 Holmdel Road, Holmdel, NJ, USA; gr@alcatel-lucent.com
[2] III-V Labs, Route de Nozay, Marcoussis, France; [3]University of California, Davis CA USA

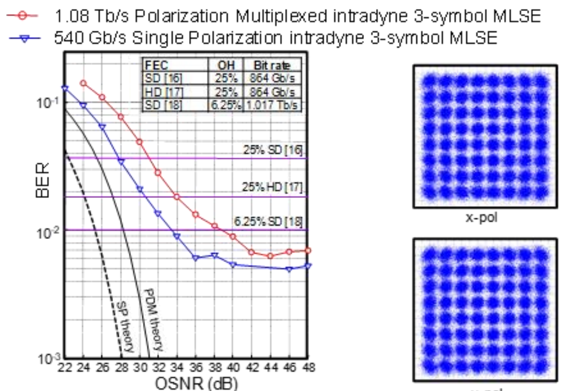
IEEE Photonic Conference (IPC), Virginia, USA, 2015

First demonstration of single carrier all-ETDM 1-Terabit transmitter

1-Terabit 90-Gbaud PDM 64-QAM experiment

12 x 45 Gb/s data signals





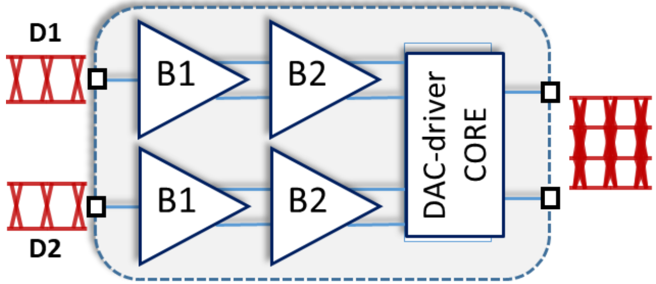
[10] L. M. Zhang, et. al., Journ. Lightw. Technol. vol. 32, p. 1999, (2014).
[11] Y. Kou, et. al., IEEE Transac. Info. Theory, vol. 47, p. 2711, (2001).
[12] L. Schmalen, et. al., Proc. of SPAWC, Stockholm, p. 460, (2015).

BER measurements and constellations

First demonstration of single carrier all-ETDM 1-Terabit transmitter

PAM-4 DAC-driver with large output swing

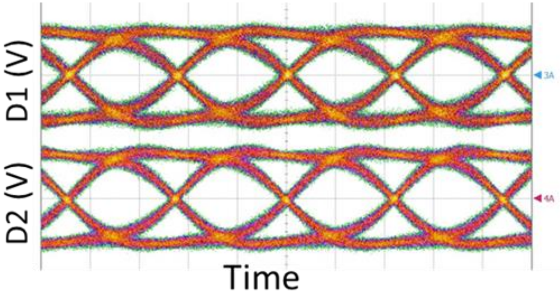
- Circuit from Power-DAC family
- DAC architecture
  - Clockless architecture; NRZ input data must be retimed
  - B1 block – SE to diff conversion
  - B2 block – preamplificaton
  - DAC-driver core provides DA conversion and amplification



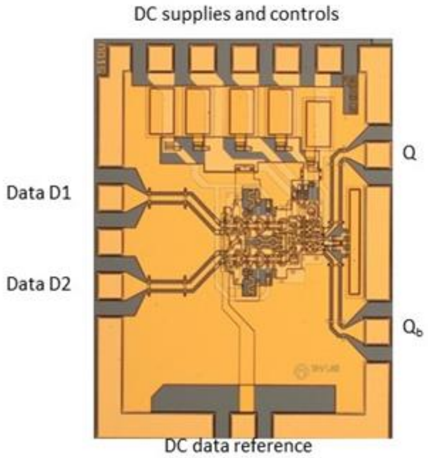
- Design objective
  - Realize the highest combination of PAM-4 symbol-rate and output swing

Particularity : Circuit fabricated at III-V Lab using InP/GaAsSb epitaxy grown at ETH-Z

Measurements 90-Gbaud PAM-4 with 5.5 V_{ppdiff} output

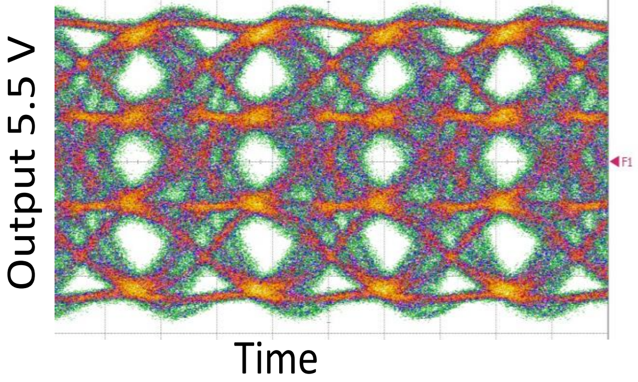


Eye amplitude/height
- D1 362/185 mV
- D2 380/227 mV



Footprint	1.2x1.5 mm^2
Circuit core	0.52x0.47 mm^2
37 transistors	

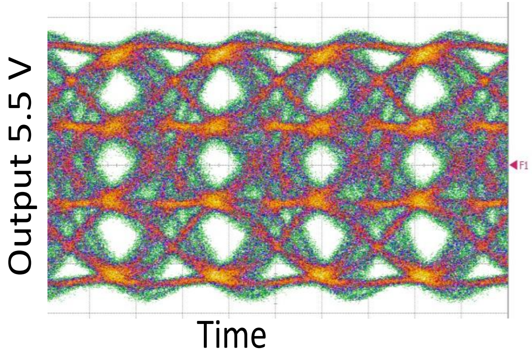
5.5 V_{ppdiff} 90 Gbd (180 Gb/s)



High quality and 5.5-V_{ppdiff} 90 GBd PAM-4 signal generation

90 Gbaud and 112 Gbaud measurements

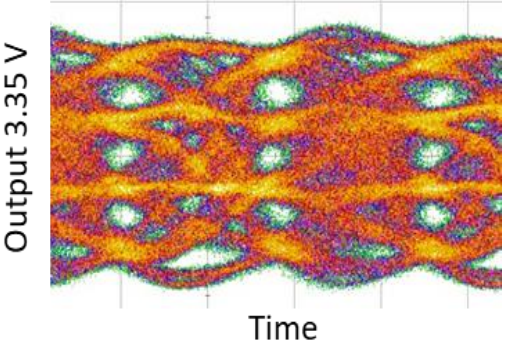
90 Gbaud (180 Gb/s)



Power consumption 1W
Over 12-dB gain control

FoM= 3.1 GBd

112 Gbaud (224 Gb/s)



Power consumption 0.6W

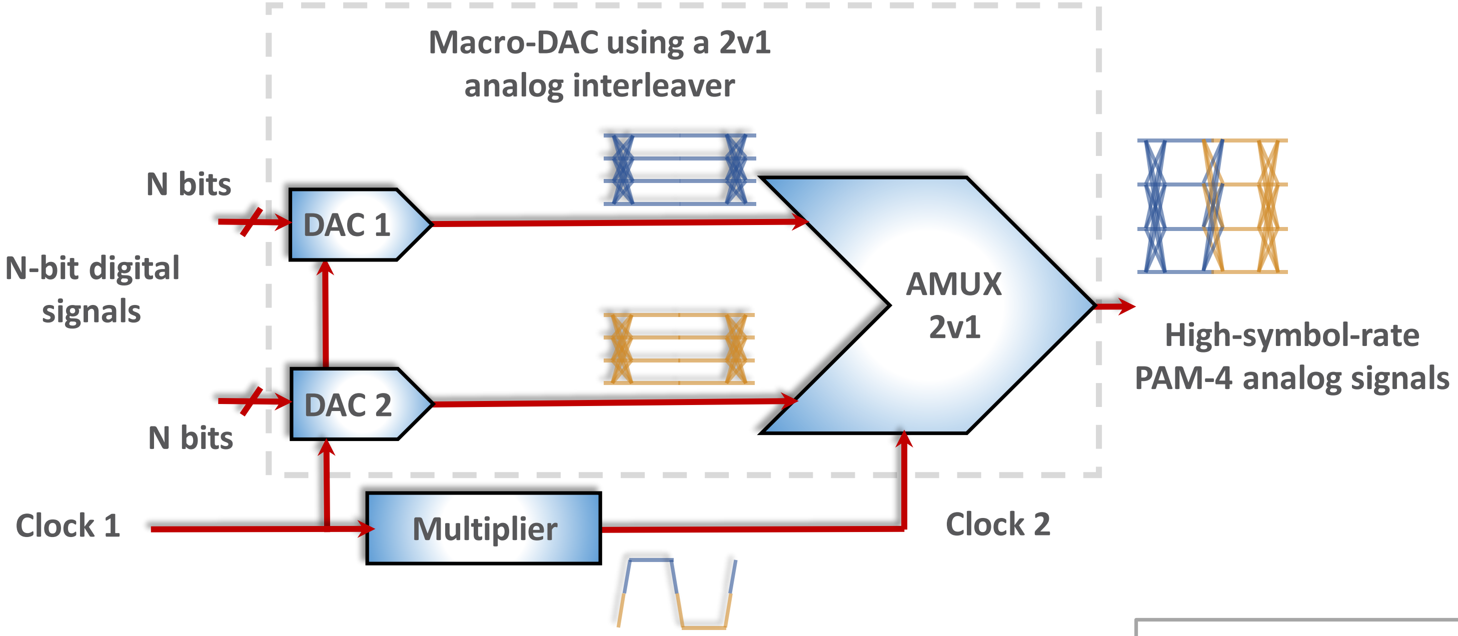
FoM= 2.6 GBd

$$FoM_{driver} = D_S \cdot \frac{V^2_{s\ ccdiff}}{8.Z_0.P_{DC}}$$

- D_S: PAM-4 symbol-rate
- $V_{s\ ccdiff}$: Output swing at D_S
- Z_0: Load impedance
- P_{DC}: Total DC power consumption

InP-DHBT DAC-driver with record FoM at 90 and 112 GBd in PAM-4

Analog Interleaver (AMUX) principle of operation



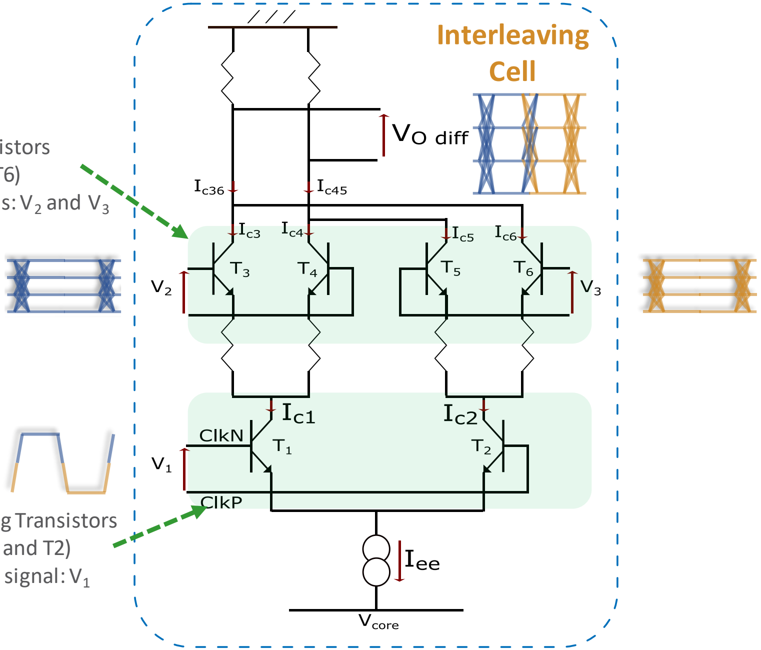
AMUX : Analog Interleavers
2v1 : Two-to-one

Interleaving of 2 DACs to double the overall bandwidth

2v1 analog interleavers: interleaving cell principle

❖ Analog interleaving cell operation

Data transistors
(T3 to T6)
Data input signals: V_2 and V_3



Switching Transistors
(T1 and T2)
Clock signal: V_1

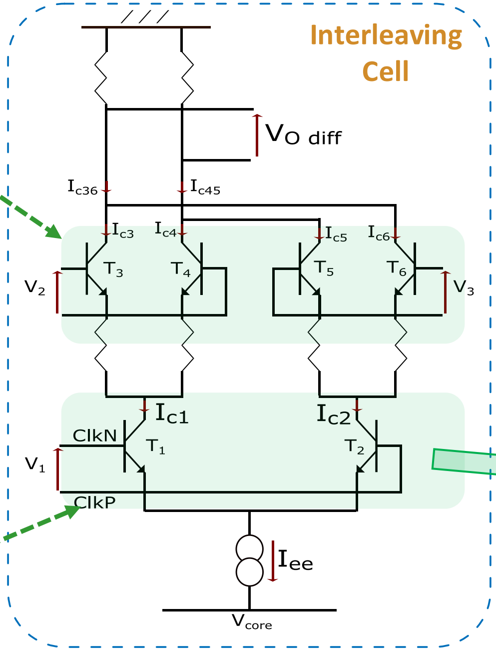
InP DHBT are key for conjugated high-speed and high linearity

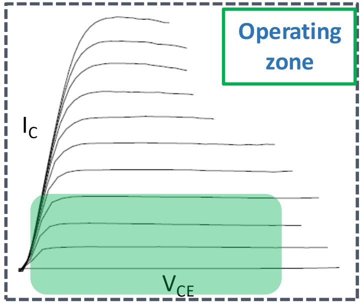
2v1 analog interleavers: interleaving cell principle

Analog interleaving cell operation

Data transistors
(T3 to T6)
Data input signals: V_2 and V_3

Switching Transistors
(T1 and T2)
Clock signal: V_1





High current switching speed: f_T

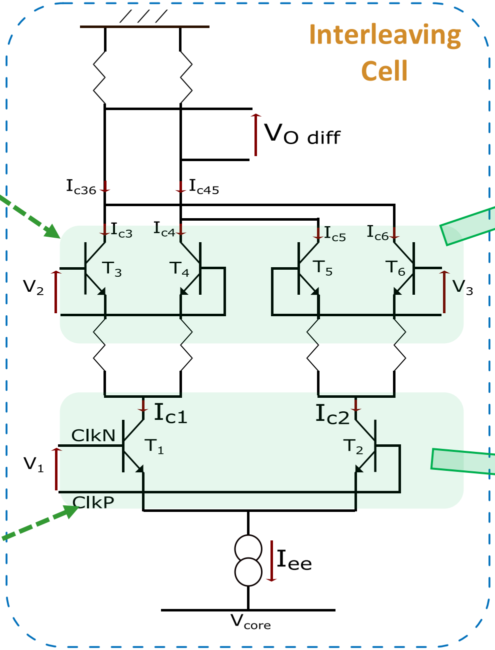
InP DHBT are key for conjugated high-speed and high linearity

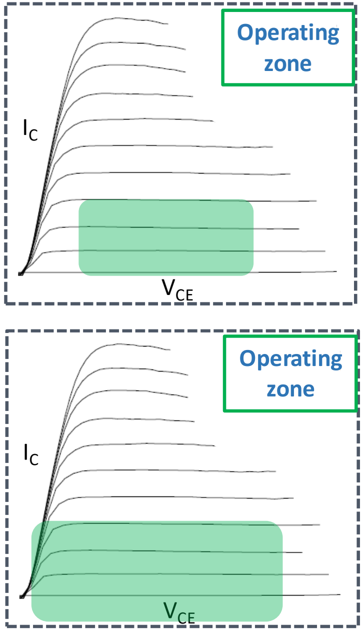
2v1 analog interleavers: interleaving cell principle

Analog interleaving cell operation

Data transistors
(T3 to T6)
Data input signals: V_2 and V_3

Switching Transistors
(T1 and T2)
Clock signal: V_1





High linearity
+
High speed: f_T & f_{MAX}

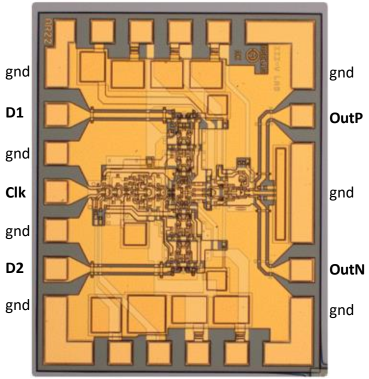
High current switching speed: f_T

InP DHBT are key for conjugated high-speed and high linearity

InP DHBT AMUX running up to 160 GSa/s

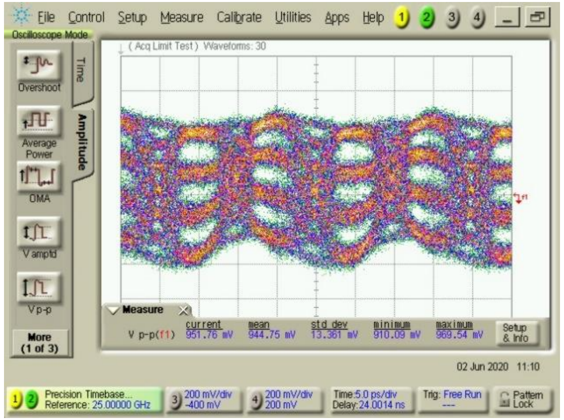
AMUX

InP DHBT AMUX

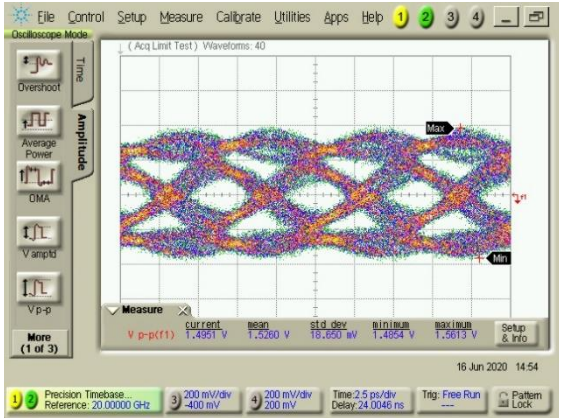


Die size: 1.2x.1.5 mm²
Core size: 0.6x0.6 mm²

0.95 V_{ppdiff} at 100 GBd (200 Gb/s)



1.5 V_{ppdiff} at 160 GBd (160 Gb/s)

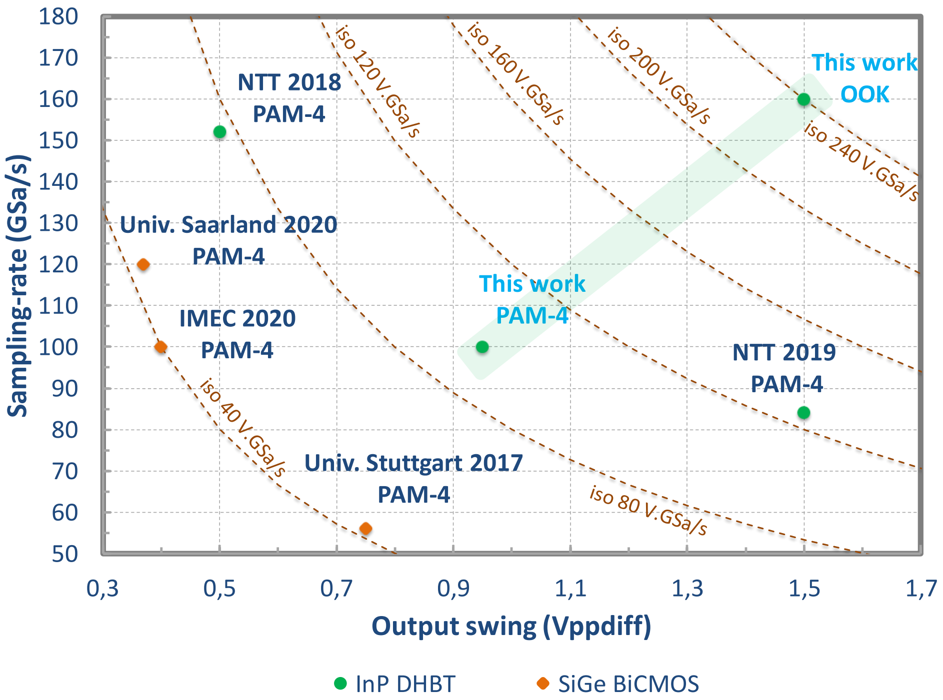


Power consumption: 0.94 W

R. Hersent et al., "Analog-multiplexer (AMUX) circuit realized in InP DHBT for high order electrical modulation format (PAM-4, PAM-8)" 2020 IEEE MIKON Conference, 2020

Up to 160 GSa/s sampling-rate operation with large output swing

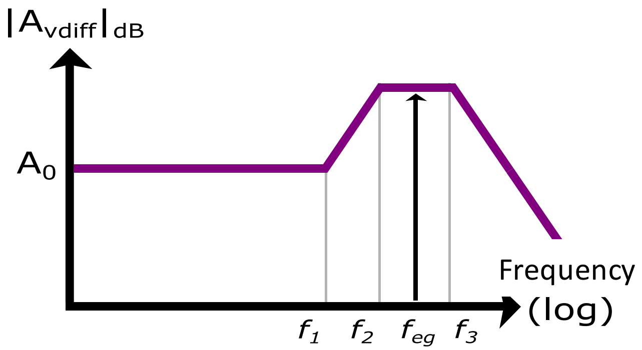
High-symbol-rate analog interleavers' state-of-the-art



Highest sampling-rate x output swing FoM in current state-of-the-art

Linear equaliser-driver to compensate bandwidth limitations

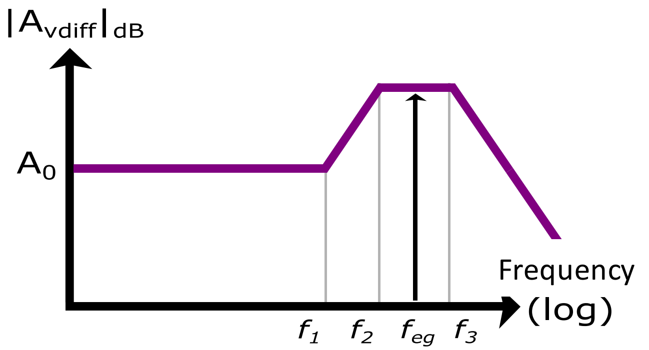
Linear equaliser-driver principle

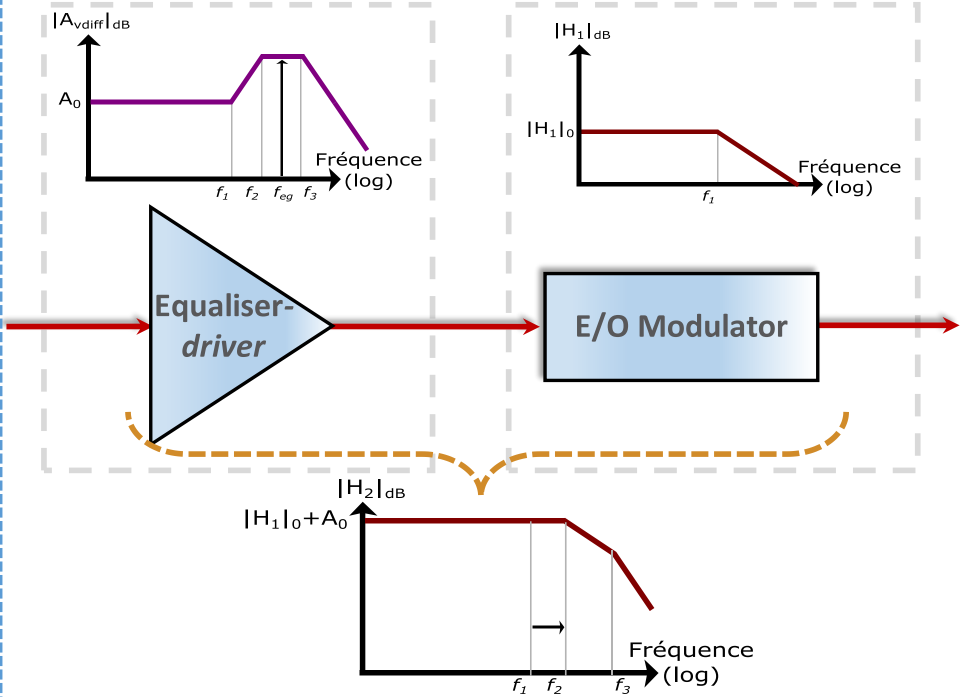


Linear equaliser-drivers can compensate for E/O modulators' bandwidth limitations

Linear equaliser-driver to compensate bandwidth limitations

Linear equaliser-driver principle

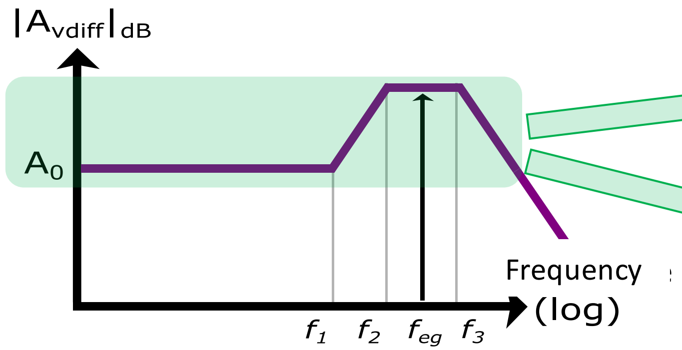




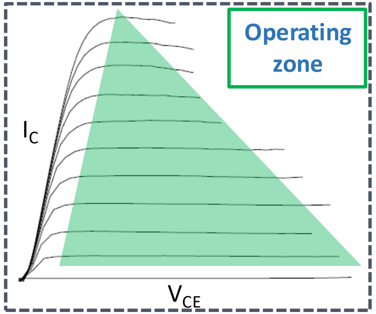
Linear equaliser-drivers can compensate for E/O modulators' bandwidth limitations

High-performance InP DHBT to empower linear eq.-driver

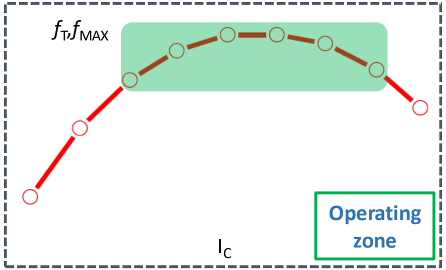
Linear equaliser-driver principle



❖ High-speed + high linearity + high output power



High linearity + High output power

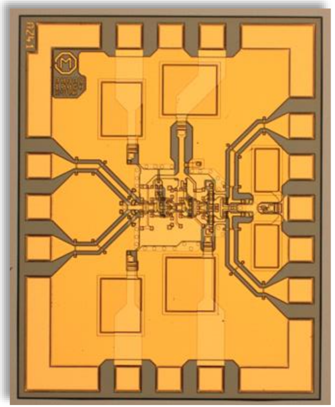


High-speed

Conjugating large bandwidth and large linear output swing operation requires to find the sweet spot

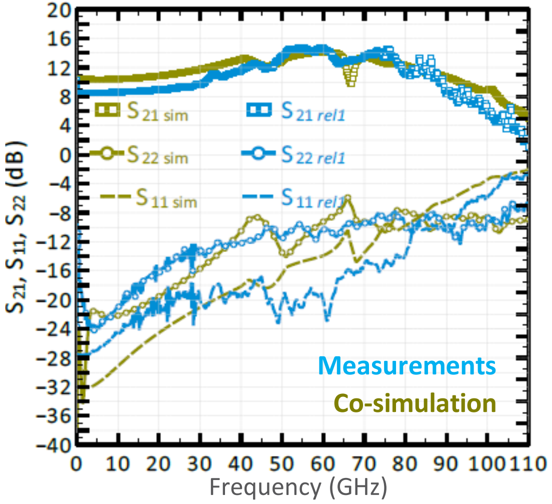
InP DHBT linear equaliser-driver 80-GBd (160-Gb/s) PAM-4

InP DHBT linear equaliser-driver

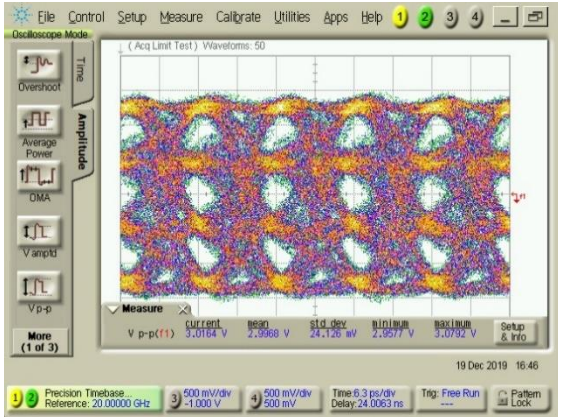


Die size: 1.2x1.5 mm²
Core size: 0.2x0.6 mm²

106 GHz bandwidth
6 dB peaking gain



3-V_{ppdiff} at 80 GBd (160 Gb/s)

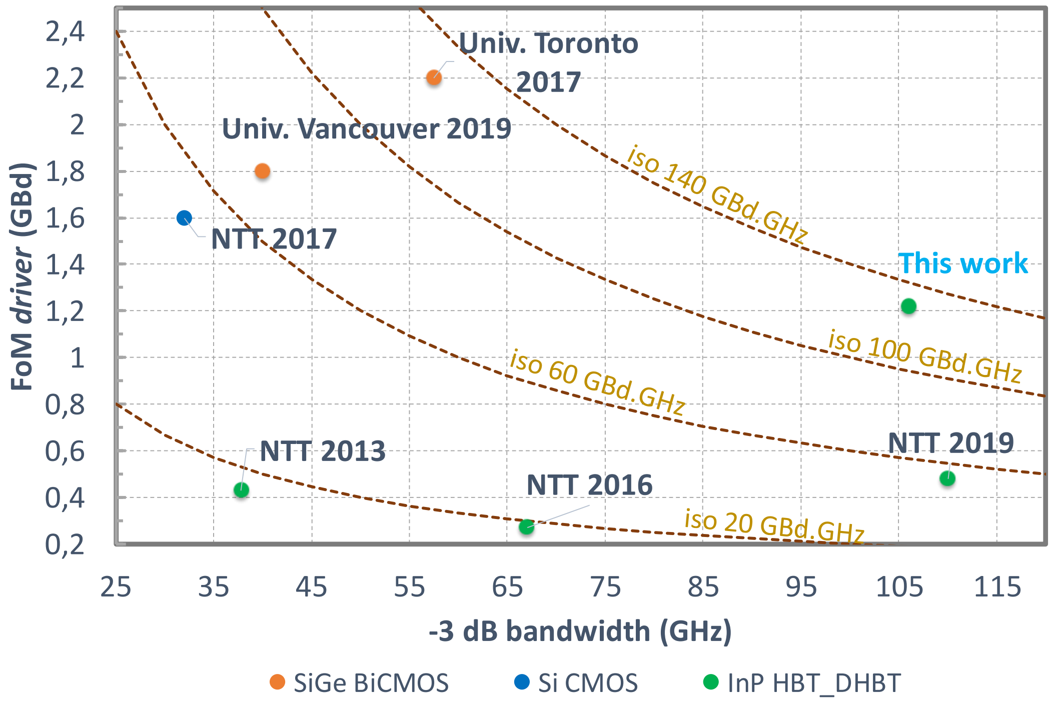


Power consumption: 0.74 W

R. Hersent et al. "106-GHz bandwidth InP DHBT linear driver with a 3-Vppdiff swing at 80 GBd in PAM-4",Electronics Letters, pp. 1-2, April 2020. doi: 10.1049/el.2020.0654

A 3-$V_{pp\ diff}$ linear output swing at 80 GBd in PAM-4 with 106 GHz bandwidth and 6-dB equalisation gain

Linear equaliser-driver state-of-the-art



$$FoM_{driver} = D_S \cdot \frac{V^2_{s\ ccdiff}}{8.Z_0.P_{DC}}$$

D_S: PAM-4 symbol-rate

$V_{s\ ccdiff}$: Output swing at D_S

Z_0: Load impedance

P_{DC}: Total DC power consumption

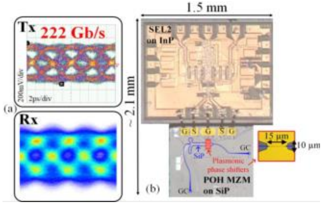
A 1.22-GBd efficiency in PAM-4 at 80 GBd: state-of-the-art performances yet missing higher symbol-rate measurements

Conclusions

- InP DHBT technologies provide ultra high performances to fill the gap towards higher symbol-rate transmissions and optical capacity
- III-V Lab's technology provides among the highest performances in the state-of-the-art
- III-V Lab InP-DHBT based digital and analog circuits show state-of-the-art and beyond performances with conjugated large-output-swing with high bandwidth/speed

Thank you !!!

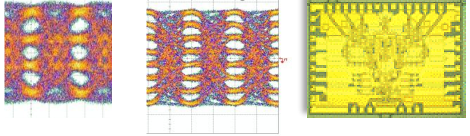
Ultra-high speed digital Mux



*Mardoyan H. et al, **222-Gbaud** on-off keying transmitter using ultra-high-speed **2:1 selector** and plasmonic modulator on silicon photonics, OFC PDP 2019*

High symbol rate large swing DAC

84-GBd 3.7-V_{ppdiff} PAM-4 **50-GBd 4.2-V_{ppdiff} PAM-8**



*A. Konczykowska et al. "**Extreme speed power-DAC** leveraging InP DHBT for ultimate capacity single-carrier optical transmissions", Journal of lightwave Technology, 2017*

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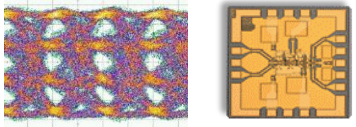
High symbol rate large swing linear driver

80-GBd 3-V_{ppdiff} PAM-4



*R. Hersent et al. "**106-GHz** bandwidth InP DHBT linear driver with a **3-V_{ppdiff} swing at 80 GBd** in PAM-4", IET Electronics Letters, 2020*

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